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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/788,525 | 02/26/2004 | Ignazio Martines | 61181-00014USPX | 6880 |

23932 7590 12/07/2005

JENKENS & GILCHRIST, PC
1445 ROSS AVENUE
SUITE 3200
DALLAS, TX 75202

| EXAMINER | |
|---|---|
| LE, TOAN K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/788,525 | MARTINES ET AL. | |
| | Examiner | Art Unit | |
| | Toan Le | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/21/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: East search history.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. This office acknowledge receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on July 21, 2004.

3. Information disclosed and list on PTO 1449 was considered.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Tassan Caser et al. (US. 5,822,247).

Regarding claims 1-6, Tassan Caser et al. disclose in Figs. 3, 4, 5 and 7, a gate voltage regulation system for the programming and/or soft programming phase of non volatile memory cells, wherein the memory cells being organized in cell matrices with corresponding circuits responsible for addressing, decoding, reading, writing and erasing the memory cell content (see

col. 1, lines 11-33), comprising: Charge pump voltage regulators (14) for biasing gate terminals of the cells in the programming phase with a predetermined voltage value (see table 1 in col. 5); a first regulation stage (15, 23) including a charge pump (15) supplied with a supply voltage (see col. 4, lines 24-26) and regulated by means of a stable voltage regulator (23, see col. 4, lines 48-49), and a second regulation stage (68, 27), being structurally independent (see fig. 3), responsible for the programming phase and soft programming phase , respectively, the first stage generating a supply voltage (hv) for said second stage (See fig. 3), wherein the second stage (68) comprises: a current mirror structure (see fig. 5) with an output stage comprising a transistor (M14 of fig. 5), a circuit branch of the current mirror structure comprises a current mirror structure disabling transistor (M9 of fig. 5) controlled by a programming phase (program) and operating in a saturation status (see col. 7, lines 25-30), and an output (36 of figs. 3, 7) being coupled to the gate terminals of the cells (see col. 5, lines 4-10).

Regarding claims 7-12, Tassan Caser et al. disclose in Figs. 3, 4, 5 and 7, a circuit comprising: a first voltage regulation stage (15, 23) generating a voltage ramp output (hv) at a first output (18); a second voltage regulation stage (27) generating a regulates voltage output (Vxreg) at a second output (36) which is couple to the gate terminals of volatile memory cells or floating gate memory cells (see col. 5, lines 4-10 and col. 1, lines 5-15) wherein the first output (18) of the first voltage regulation stage is a power supply for the second voltage regulation stage (see fig. 3); and a select switch (M11, M12 of fig. 5) responding to a control signal (PROGHN) to selectively connect the first output (18) to the second output (36, see fig. 3 and col. 7, lines 57-60). Tassan Caser et al. further disclose the control signal (PROGHN) having first value activating the selection switch to apply the voltage ramp output to the gates terminals of plurality

of memory cells for programming, and a second value de-activating the selection switch to apply the regulated voltage output to the gate terminals of the plurality of memory cells for soft programming (see col. 7, lines 58-64).

Regarding claims 13-19, Tassan Caser et al. disclose a circuit comprising: a plurality of volatile memory cells, each including a floating gate transistor, each of the transistors sharing a common gate connection (see col. 1, lines11-16); and a gate voltage regulator circuit (14 of fig. 3) having an output coupled to the common gate connection (see col. 7, lines 4-8) and receiving a programming control signal (program), the gate voltage regulator circuit comprising: a first regulator (15, 23 of fig. 3) having a first output (18) and generating a programming ramp voltage (hv); a second regulator (27) having a second output (36) and generating a soft programming voltage (vxreg) wherein the first output (18) is a power supply for the second regulator (see fig. 3); and a selection circuit (68 of figs. 3 and 5) responsive to the programming control signal (program and proghn) for applying the programming ramp voltage to the common gate connection in a first operating mode and applying only the soft programming voltage to the common gate connection in a second operating mode (see col. 7, lines 11-64) wherein the selection circuit (68) comprises a switch circuit (44 of fig. 5) that selectively connects the first output to the second output (see fig. 5) having a transistor which has its conduction terminal coupled between the first and second outputs (see fig. 5) and its control terminal coupled to receive the programming control signal (see fig. 5). Tassan Caser et al. further disclose the selection circuit (68) absorbing voltage changes in the programming ramp voltage when in the second operating mode so as to allow a substantially constant current to be supplied with the soft programming voltage, and permitting voltage changes in the programming ramp voltage to be

applied to the common gate connection when in the second operating mode (see line 64 of col. 6 to line 64 of col. 7).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yachareni et al. (US. 6,493,266) disclose method and systems for verifying an erased cell threshold voltage of one or more dual bit cells in a flash memory.

Trinh et al. (US. 5,777,926) disclose a circuit providing programming, erasing, and reading voltages to a floating memory cells.

Kowshik et al. (US. 5,687,116) disclose a programming pulse ramp control circuit.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Le whose telephone number is (571) 272-1872. The examiner can normally be reached on M-F (8.00AM - 5.30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TL
December 01, 2005

ANH PHUNG
PRIMARY EXAMINER